REMARKS

This Application has been carefully reviewed in light of the Official Action mailed November 23, 2001. In order to advance prosecution of this Application, Claims 1, 5, 6, 11, and 17 have been amended. Applicant respectfully requests reconsideration and favorable action in this case.

Claims 1, 2, 4-15, and 17-19 stand rejected under 35 U.S.C. §102(b) as being anticipated by Amini, et al. With respect to Independent Claim 1, there is recited ". . . enabling a switch associated with the selected request to provide access to the bus in response to the control signal." By contrast, the Amini, et al. patent provides no disclosure with regard to a method of providing access to a bus by enabling a switch as provided in the claimed invention. Support for the above recitation can be found at page 6, line 28, to page 7, line 4, of Applicant's specification. Therefore, Applicant respectfully submits that Claims 1, 2, and 4-10 are not anticipated by the Amini, et al. patent.

With respect to Independent Claim 11, there is recited ". . . a plurality of enabling switches on the bus, each enabling switch coupled to a corresponding processing device, each enabling switch providing the corresponding processing device with access to the bus in response to a control signal from the bus controller." By contrast, the Amini, et al. patent discloses a system wherein devices are granted access to the bus via grant lines that are direct connections between the devices and the controller. See Col. 8, lines 65-68, of the Amini, et al. patent. Thus, the Amini, et al. patent has no disclosure with respect to the use of enabling switches as provided in the claimed invention. Therefore, Applicant respectfully submits that Claims 11-15 are not anticipated by the Amini, et al. patent.

With respect to Independent Claim 17, there is recited, ". . . a plurality of pass transistors, each pass transistor operable to provide an associated processing device with bus access, each pass transistor operable to receive a control signal to enable and disable bus access for the associated processing device." By contrast, the Amini, et al. patent discloses access to the bus is controlled by direct connections between the device and the bus controller. See Col. 8, lines 65-68, of the Amini, et al. patent. Thus, the Amini, et al. patent has no disclosure with respect to a bus comprised of a plurality of pass transistors operable to enable and disable bus access for associated processing devices as provided in the claimed invention. Therefore, Applicant respectfully submits that Claims 17-19 are not anticipated by the Amini, et al. patent.

The Examiner has only provided a general rejection of the claims without showing how each and every element of each and every claim are shown in the Amini, et al. patent. Applicant respectfully requests the Examiner to provide a proper and complete examination of this Application by showing how each and every element of each and every claim, including the dependent claims, might be disclosed by the prior art.

Claims 3, 16, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Amini, et al. Independent Claim 1, from which Claim 3 depends, Independent Claim 11, from which Claim 16 depends, and Independent Claim 17, from which Claim 20 depends, have been shown above to be patentably distinct from the Amini, et al. patent. Therefore, Applicant respectfully submits that Claims 3, 16, and 20 are patentably distinct from the Amini, et al. patent.

Applicant has now made an earnest attempt to place this case in condition for allowance. For the foregoing reasons

and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-20.

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,

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MARKED UP VERSION OF SPECIFICATION AND CLAIM AMENDMENTS

For the convenience of the Examiner, all claims have been presented whether or not an amendment has been made. The specification and claims have been amended as follows:

IN THE CLAIMS

1. (Amended) A method of providing access to a bus, comprising:

receiving a request for access to the bus;

selecting the request according to a priority associated with the request;

generating a control signal in response to selection of the request;

enabling a switch associated with the request to provide access to the bus [associated with the selected request] in response to the control signal.

2. The method of Claim 1, wherein the bus is a PCI bus.

3. The method of Claim 2, wherein the PCI bus operates at a frequency of at least 66 MHZ.

4. The method of Claim 1, wherein the request is received from a device desiring to communicate over the bus.

5. (Amended) The method of Claim 1, further comprising:

receiving a plurality of access requests for the bus, each of the plurality of access requests being received from one of a plurality of devices coupled to the bus, each of the plurality of devices having a switch associated therewith;

selecting a particular one of the plurality of access requests according to a predetermined priority protocol;

generating a control signal corresponding to the selected particular one of the plurality of access requests;

providing the control signal to a particular one of the plurality of devices that sent the selected particular one of the plurality of access requests, the control signal enabling the switch associated with the particular one of the plurality of devices to provide access to the bus.

6. (Amended) The method of Claim 5, further comprising:

selecting a next one of the plurality of access requests according to the predetermined priority protocol;

generating a control signal corresponding to the selected next one of the plurality of access requests;

providing the control signal to a next one of the plurality of devices that sent the selected next one of the plurality of access requests, the control signal enabling the switch associated with the next one of the plurality of devices to provide access to the bus prior to an end of access to the bus for the particular one of the plurality of devices.

7. The method of Claim 6, further comprising:

determining an end of access to the bus for the particular one of the plurality of devices;

initiating access to the bus by the next one of the plurality of devices in response to the end of access to the bus for the particular one of the plurality of devices.

8. The method of Claim 7, further comprising:

generating a disabling control signal in response to the end of access to the bus for the particular one of the plurality of devices;

preventing the particular one of the plurality of devices from accessing the bus in response to the disabling control signal.

9. The method of Claim 1, further comprising:

limiting a number of generated control signals in order to control a load on the bus.

10. The method of Claim 1, further comprising:

generating a disable control signal for a request not selected in order to disable access to the bus.

11. (Amended) A system for providing access to a bus, comprising:

a bus controller;

a plurality of processing devices coupled to the bus controller by a bus;

a plurality of enabling switches on the bus, each enabling switch coupled to a corresponding processing device, each enabling switch providing the corresponding processing device with access to the bus [for its corresponding processing device] in response to a control signal from the bus controller.

12. The system of Claim 11, wherein the bus controller allows simultaneous access to the bus by a predetermined number of the plurality of processing devices in order to limit a load on the bus.

13. The system of Claim 11, wherein the bus controller receives a plurality of access requests from the plurality of processing devices for access to the bus.

14. The system of Claim 13, Wherein the bus controller arbitrates the plurality of access requests from the plurality of processing devices according to a predetermined protocol.

15. The system of Claim 11, wherein the bus is a PCI bus.

16. The system of Claim 15, wherein the PCI bus operates at a frequency of approximately 66 MHZ.

17. (Amended) A PCI bus, comprising:

a plurality of pass transistors, each pass transistor operable to provide an associated processing device with bus access [for an associated processing device], each pass transistor operable to receive a control signal to enable and disable bus access for its associated processing device.

18. The PCI bus of Claim 17, wherein a particular pass transistor receives an enable control signal in response to an access request sent by its associated processing device.

19. The PCI bus of Claim 17, wherein a particular pass transistor is operable to disable bus access for its associated processing device such that the particular processing device does not appear to be coupled to the PCI bus.

20. The PCI bus of Claim 17, wherein each of the processing devices is operable to communicate at a 66 MHZ rate.